Using Design Based Binning to Improve Defect Excursion Control for 45nm Production

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***Abstract*- For advanced device (45 nm and below), we proposed a novel method to monitor systematic and random excursion. By integrating design information and defect inspection results into automated software (DBB), we can identify design/process marginality sites with defect inspection tool. In this study, we applied supervised binning function (DBC) and defect criticality index (DCI) to identify systematic and random excursion problems on 45 nm SRAM wafers. With established SPC charts, we will be able to detect future excursion problem in manufacturing line early.**

INTRODUCTION

For the 45 nm node, immersion litho has been a major enabling technology for pattern shrinkage. Litho R&D engineers have applied OPC and tighter process windows to mitigate the impact from decreasing pitch and complex pattern design. However, pattern-related systematic yield loss is still listed as a major barrier for 45 nm advancement to production. Certain pattern designs are sensitive to process variation from film deposition, photo and etch steps. A combination of film over-deposition and under-etching at these patterns can lead to film residue, in the form of line bridging defects (Fig. 1).

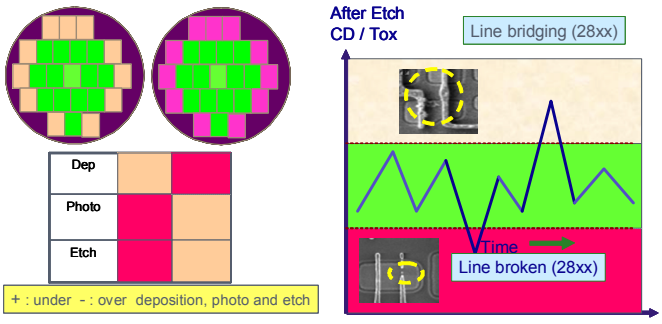

Figure 1. Marginal design problem and process variation can lead to systematic excursion events

This problem will get worse in the production stage, with process variation arising from multiple tools and modules. With sensitive inspection tools and small pixel inspection recipes, pattern excursions can be identified. However, if the failed pattern count is low (in tens) and the total defect count is high (in thousands), current random sampling methods (sampling 50 to 100 defects per wafer) can easily miss this excursion, with potentially significant consequences in terms of yield, time to market and profit.

To address this issue, we have proposed a different methodology that employs novel software (Design Based Binning) to bin the defect of interest with its pattern background information. For each defect, the inspection results are compared against the design layout to identify defects occurring at certain design locations. (Fig. 2)

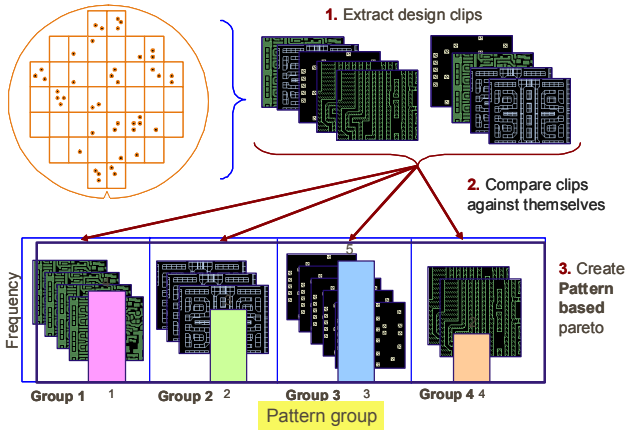

Figure 2. Design based binning method: taking design and inspection information to identify potential systematic pattern problem

For known systematic pattern problem, even this might be fixed with design/OPC modification. This can still show up as excursion problem and needs to be constantly monitored. We can bin and track for its occurrence with DBC (Design Based Classification Fig. 3)

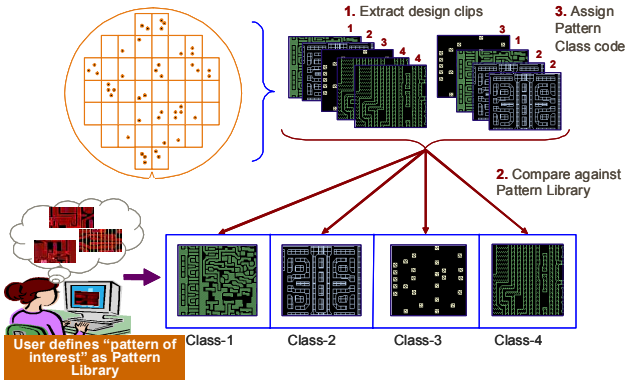

Figure 3. DBC: Supervised binning methodology help detect known systematic excursion

For random excursion, we can also use design and pattern information to monitor. We merge defect pattern background and defect size information into a propriety model, this model will automatically calculate and generate an index from 0 to 1 for each defect to indicate its criticality (Fig. 4).

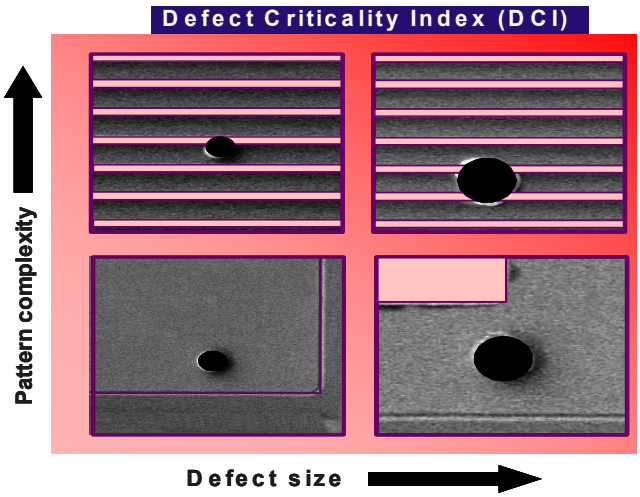

Figure 4. DCI: Random defect management using Design and defect size information

By applying DBC and DCI to inspection results, we can build SPC charts (DBC and DCI) to monitor systematic and random excursion. During the R&D stage, we can identify marginal pattern sites from either the design library or PWQ/FEM data. These risky pattern features will be built into a Design Based Library, and passed to production for monitoring. When a pattern excursion happens during a Pilot/ Production stage, the SPC chart will flag the problem. This will trigger additional defect sampling and review for specific pattern problem. This methodology will enable us to take prompt corrective action at an early stage of the excursion, before the problem is out of control.

EXPERIMENTAL DATA AND RESULTS

Wafer, inspection and defect binning

We selected four SRAM wafers from the same lot which were processed through Gate etch layer. These wafers were inspected by Brightfield inspection tool (KLA28xx) and around 50 defects were randomly sampled with review SEM. Manual classification on these reviewed defects was done and normalization of defect type was followed to check for excursion. The results from Fig. 5 indicated potential random excursion from wafer 3 and 4 as well as systematic problem (type B) from wafer 4. However, due to limited sampling defect (average 42) and high defect counts, the excursion signal was not clear in indicating the extent of problem.

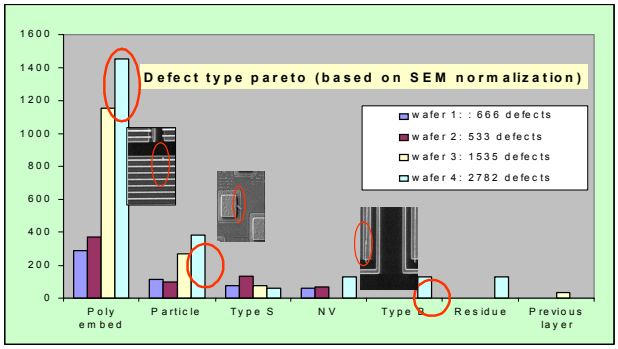

Figure 5. Traditional method for review sampling and normalization

DBC and DCI Results

Results from these four wafers were binned with DBB. One example of DBB binning results from wafer #4 was shown in Fig. 6. The top bin in the chart was from defect on dummy pattern area

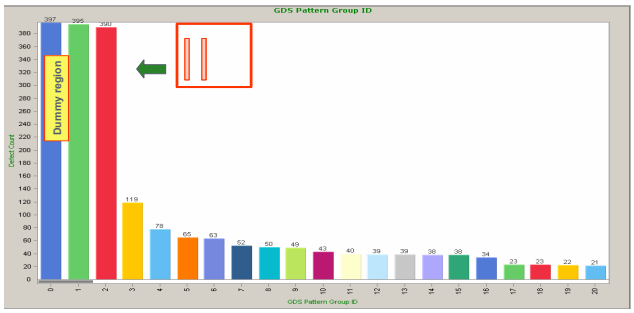

Figure 6. DBB: un-Supervised binning results on wafer #4. Top Pareto bin is defect on dummy pattern

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tern regions; this is regarded as "don't care" region and can be filtered out with no impact to yield decision. By running DBC analysis on all wafers, we found one pattern type from hot spot library had high defect count on wafer 4 compared with others (Fig. 7). This wafer was sent for further SEM review and the outcome was confirmed as systematic excursion issue.

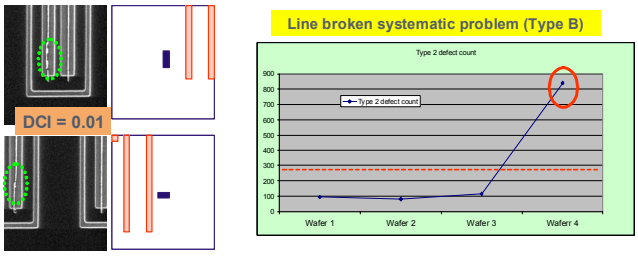

Figure 7. DBC binning results shown wafer #4 had systematic excursion as in the SEM pictures

DCI results for random excursion monitoring For each defect, DCI was calculated (range from 0 to 1) automatically by DBB software. The lower index indicates that this defect to be less critical and the results can help defect review prioritization decision. Example of DCI number and corresponding defect pictures were Fig. 8. To protect customer IP, GDS clip was hand drawn and its scale does not reflect its original design.

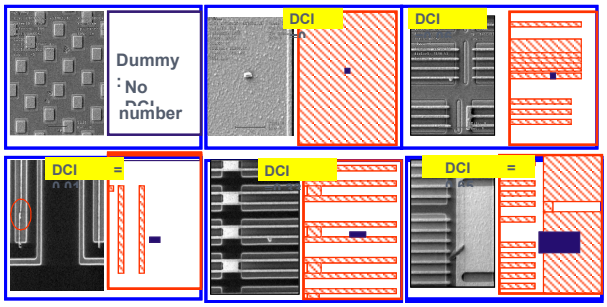

Figure 8. DCI samples shown defect size and pattern background information

Based on SEM review and DCI number, we decided that we can put a threshold number of 0.1 for non-critical random defect (small defect on spare pattern background). Based on this, we monitored the percentage of non-critical defect count (DCI < 0.1) and plotted the chart. From the results it indicated that wafer #3 has higher percentage of critical random defect. This triggered review sampling on defect group with higher DCI. From SEM review, we identified polymer excursion defect which was missed from traditional sampling method. The results were shown in Fig. 9.

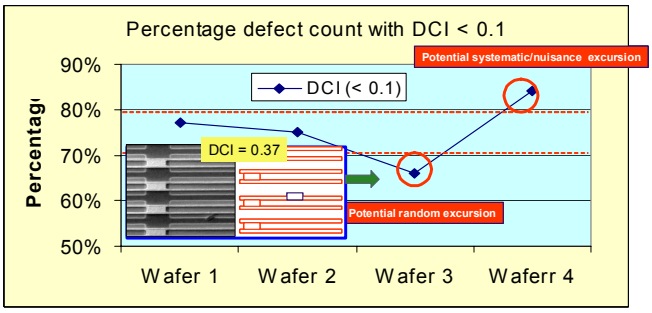

Figure 9. DCI chart shown wafer # 3 had potential random excursion as in SEM picture

SUMMARY

We summarized the comparison between DBB methodology and current UMC practice in table 1.

From many use cases in UMC, DBB has shown benefits in finding pattern-related defects on 45 nm device wafers. This is a novel method to find systematic defects and has the potential to serve as the in-line monitor for systematic and random excursion as shown in this paper.

TABLE 1
UMC current practice and DBB method comparison

Item	Current Practice	New DBB Methodology
Defect on Dummy	Many defects on dummy pattern	0 %
Nuisance (Poly grain/cap, small particle/field)	Vary/high defect count	Use DCI < 0.1 to screen out random non-DOI
Systematic defect (pattern failure) identification	Repeater analysis Review same type > 2	Control chart on "known pattern of interest (POI)"
Excursion trigger	By total defect counts Bad die%	By count and DCI percentage (i.e. for DCI < 0.1)
SEM Review sampling 50 defects	Random selection	Systematic defect with DBC and random review with high DCI

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